Improved free-running InGaAs/InP single-photon avalanche diode detectors operating at room temperature

R.E. Warburton, M.A. Itzler and G.S. Buller

Room-temperature operation of InGaAs/InP single-photon avalanche diode detectors operating in free-running mode, with no electrical gating, is demonstrated. An improved design of device structure permitted significantly lower dark count rates than previously reported. Free-running operation at room temperature using an incident wavelength of 1550 nm gave a noise equivalent power of 1.5×10^{-15} $WHz^{-1/2}$ with improved photon timing jitter.

InGaAs/InP single-photon avalanche diode detectors (SPADs) are favoured in a number of applications for single-photon detection at wavelengths around 1550 nm, e.g. quantum key distribution (QKD) [1]. Gated quenching, in various guises, including the use of active quenching circuits [2], has been implemented in many of these applications to limit the charge flow per event to reduce the detrimental effects of the afterpulsing phenomenon. This has permitted gating frequencies greater than 1 GHz and high count-rates at the expense of gate 'on' times. For applications such as time-resolved photoluminescence and time-of-flight laser ranging [3] long 'on' periods are required to most efficiently extract the information about the sample, or target, respectively. Ideally, a free-running detector [4] would be preferred for such applications. Recently, we reported the use of a Princeton Lightwave Inc. (PLI) InGaAs/InP SPAD employing passive quenching at low excess biases [5] which illustrated the first report of an InGaAs/InP SPAD operating free-running at room temperature. In this work, different characteristics of device performance can be exploited depending on the choice of quenching resistor; the lower Rs the faster the recharging of the diode after an avalanche event, however with a greater Rs a higher bias could be applied resulting in higher single-photon detection efficiency (SPDE) and lower photon-timing jitter. With the first generation of PLI InGaAs/InP SPADs we were able to achieve 3% SPDE at most temperatures and a maximum count-rate of 4 Mc/s [5]. Significantly, the low dark count rates (DCR) found in these experiments meant room-temperature operation could be achieved in free-running mode with negligible effects of afterpulsing evident.

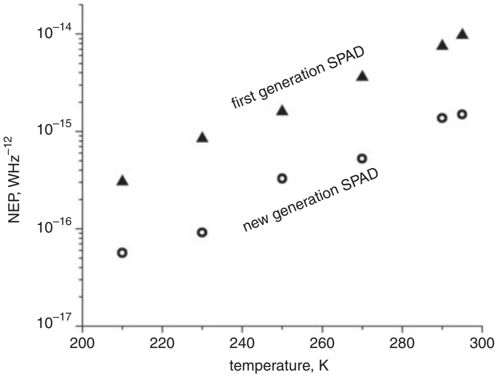

Fig. 1 *Minimum NEP at $\lambda = 1550$ nm against temperature for first and new generation InGaAs/InP SPADs operated in low excess bias passive quenching mode using 100 kΩ quenching resistor*

Recently, a new generation of 1550 nm wavelength SPAD designs was developed by PLI including negative feedback provided by the monolithic integration of a thin film resistor [6]. In the work reported in this Letter, reference samples from the same generation of devices described in [6] were used in conjunction with an external resistor to provide quenching. The SPAD design differs from that reported previously [5] in that the electric field within the InP multiplication region is designed to be significantly lower in Geiger-mode in order to suppress dark carrier generation via trap-assisted tunnelling, as modelled previously for similar InGaAsP/InP SPADs [7]. In this design the multiplication thickness was approximately 1.5 μm.

From previous work [5], we selected a 100 kΩ resistor in order to provide a good compromise in the trade-off between maximum counting rate and maximum SPDE. Noise equivalent power (NEP) was chosen as a figure of merit to compare the new generation of devices with the previous since NEP takes into account both SPDE and DCR:

$$NEP = h\nu \frac{\sqrt{2 \times DCR}}{(SPDE)}$$

where $h\nu$ represents the photon energy. Fig. 1 shows a direct comparison between the two designs over a range of operating temperatures using identical 25 μm diameter active areas.

The modifications to the device structure have resulted in a SPAD with a very low DCR, hence lowering the NEP. At 210K the NEP in free-running mode is close to that quoted for an InGaAs/InP SPAD operated in gated mode (4.5×10^{-17} $WHz^{-1/2}$ using a 4 ns gate at 10 kHz) at 200K [8]. At a given temperature, the maximum operating voltage used for characterisation depended mainly on the DCR for both devices. Since the device was free-running, at higher applied bias the DCR can reach a high level such that use of the detector becomes impractical; specifically, this limit occurs when the DCR reaches the order of the photon detection rate (given by the product of the photon flux and the SPDE). This range of practical use can be extended in gated quenching since the normalised DCR can be limited by reducing the gate length. A lower DCR device facilitates the use of higher excess biases, resulting in greater SPDE and lower photon-timing jitter, since timing jitter reduces with increasing excess bias. Throughout the temperature range a maximum SPDE of ~5 % was achievable with jitter as low as 450 ps at full-width-half-maximum (FWHM) measured. Fig. 2 represents a more in-depth evaluation of device performance at 270K showing the DCR measured at various values of SPDE for both first and new generation devices.

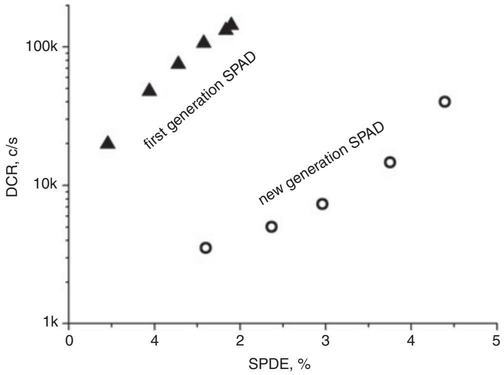

Fig. 2 *DCR against SPDE at $\lambda = 1550$ nm for first and new generation InGaAs/InP SPADs at 270K with 100 kΩ quenching resistor in series*

A critical aspect governing InGaAs/InP SPAD performance is the deleterious effects of afterpulsing [1, 5]; carriers that flow through the device during an avalanche pulse may become trapped and subsequently released after the detector is reset, causing a false event. In the free-running mode of operation reported in this Letter, the presence of afterpulsing was manifested as an increase in the background DCR with increasing count rate, as seen with the previous generation of devices at temperatures of less than 290K. However, at room temperature the reduced trap lifetime meant that the afterpulsing effects were negligible. Upon analysing the new generation design, a discernable increase in the DCR with increasing count rate was observed, even at room temperature, as shown in Fig. 3. These results were recorded at an SPDE of 2.8%, identical to the situation described previously [5]. The first generation device presented a DCR of ~1 Mc/s at 290 K, whereas at the same SPDE the new device has a DCR of ~40 kc/s. Even at the highest count rate of 1.1 Mc/s, the apparent DCR (i.e. including afterpulsing) of the new generation device is 470 kc/s – lower than that of the first generation devices. It may have been that this effect was not observed in [5] because the background was larger than the effect itself, or since the new device has a wider multiplication region (the location of the trapping centres that cause afterpulsing [2]), there will be more trapping centres present.

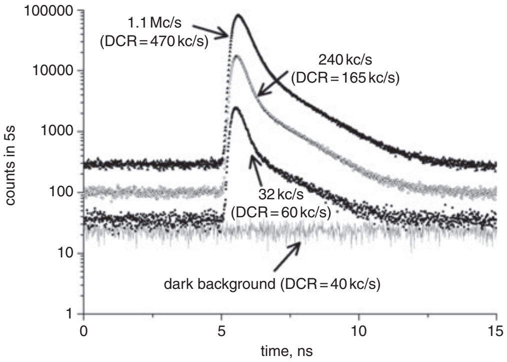

Fig. 3 *Photon counting histogram traces of new generation InGaAs/InP SPAD operated at 290 K at fixed bias at three different count rates, displayed next to each trace (DCR shown in parentheses)*

Conclusion: We have characterised an InGaAs/InP SPAD with a thick (1.5 μm) InP multiplication layer in free-running mode. Comparing this device to a previous generation device, we observed a dramatic decrease in the DCR which facilitated the use of a higher excess bias without a prohibitively high DCR. An SPDE of ∼4–5 % was achieved throughout the temperature range (210K–room temperature), with photon-timing jitter as low as 450 ps measured at FWHM. Overall, the NEP was almost an order of magnitude lower than the previous generation of devices. Future work will investigate further optimisation of the thickness of the multiplication layer for minimum NEP.

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R.E. Warburton and G.S. Buller (*School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh EH14 4AS, United Kingdom*)

E-mail: R.E.Warburton@hw.ac.uk

M.A. Itzler (*Princeton Lightwave Inc., 2555 Route 130 South, Cranbury, NJ 08512, USA*)

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